Notice of Allowability	Application No.	Applicant(s)	
	10/037,361	BYRD, JAMES M.	
	Examiner	Art Unit	
	Dipakkumar Gandhi	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/22/2005*.

2. ☒ The allowed claim(s) is/are *1-35*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Allowable Subject Matter

1. Claims 1-35 are allowed.

2. Applicant's amendment filed on 5/25/2005 has been entered.

3. The following is an examiner's statement of reasons for allowance:

The present invention pertains to error detecting systems, and more particularly, to testing error detection/correction logic. The claimed invention (claim 1 as representative) recites features such as: "...a method of testing error correction/detection logic, the method comprising: creating an initial data bit combination having n bits, wherein each data bit in the initial data bit combination has a same logical value as each other data bit in the initial data bit combination; shifting a first bit having a different logical value than the same logical value across the initial data bit combination, wherein each time the first bit is shifted, one of n data bit combinations is generated; providing each of the n data bit combinations to the error detection/correction logic; in response to said providing, the error detection/correction logic generating a set of check bits for each of the n data bit combinations; comparing the set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations."

The prior arts of record (Kurihara US 4,107,649) teaches an error detection circuit which comprises a shift register having a plurality of storing stages which sequentially shifts input data and feeds back output data from an output stage to desired ones of the stages, and a parity generator in which a parity signal is generated from the parity generator in accordance with the data storing state of the shift register, the parity signal is predicted from an initial value determined by the data storing state of the shift register in its initial state, the number of input data of logic "1" provided as an input to the shift register and/or the number of output data of logic "1" provided as an output from the shift register, and wherein the parity signal derived from the parity generator is compared with the predicted parity signal in order to detect malfunction of the error detection circuit based on the result of the comparison (col. 1, lines 44-60, Kurihara).

The prior arts, however, do not teach shifting a first bit having a different logical value than the same logical value across the initial data bit combination, wherein each time the first bit is shifted, one of n data

bit combinations is generated and provided to error detection/correction logic. The prior arts only teach that input data is shifted into the shift register. The prior arts fail to teach the error detection/correction logic generating a set of check bits for each of the n data bit combinations. The prior arts do not teach the error detection/correction logic generating a set of check bits. Instead, Kurihara's parity generator calculates the single parity bit from the input data in the shift register. The prior arts also do not disclose comparing the set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations.

Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 1 is allowable over the prior arts of record.

- Claims 2-12 are allowed because of the combination of additional limitations and the limitations listed above.
- Claim 13 recites limitations similar to those recited in claim 1. Fielder et al. only teach a program of instructions executable by a machine (col. 4, lines 60-64, Fielder et al.). Fielder et al. do not teach other limitations of claim 13. Hence, for the reasons mentioned above, claim 13 is allowable over the prior arts of record.
- Claims 14-23 are allowed because of the combination of additional limitations and the limitations listed above.
- Claim 24 recites limitations similar to those recited in claim 1. Hence, for the reasons mentioned above, claim 24 is allowable over the prior arts of record.
- Claims 25-26 are allowed because of the combination of additional limitations and the limitations listed above.
- The claim 27 recites features such as: "...a method of testing error correction/detection logic, the method comprising: providing a set of m+1 test code words to the error correction/detection logic, wherein each code word has m bits, wherein a first test code word in the set of m+1 test code words is a correct code word, wherein each test code word other than the first test code word comprises a single-bit error at a different bit position within the code word than each other test code word; in response to said providing, the error correction/detection logic decoding the set of

m+1 test code words; and verifying that the error correction/detection logic correctly decoded each of the m+1 test code words."

The prior arts of record (Kurihara US 4,107,649) teaches an error detection circuit wherein the parity signal derived from the parity generator is compared with the predicted parity signal in order to detect malfunction of the error detection circuit based on the result of the comparison (col. 1, lines 57-60, Kurihara).

The prior arts, however, do not teach a first test code word in the set of m+1 test code words is a correct code word, wherein each test code word other than the first test code word comprises a single-bit error at a different bit position within the code word than each other test code word. Kurihara's method is only concerned with comparing predicted and generated parity values. Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 27 is allowable over the prior arts of record.

- Claims 28-29 are allowed because of the combination of additional limitations and the limitations listed above.
- The claim 30 recites features such as: "...a method of testing error correction/detection logic, the method comprising: providing a set of test code words to the error correction/detection logic, wherein said providing comprises introducing an error into each of the test code words in the set by substituting check bits corresponding to an unused syndrome for a correct set of check bits within each test code word, wherein each test code word comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the set of test code words; in response to said providing, the error correction/detection logic decoding each test code word in the set of test code words; and verifying that the error correction/detection logic correctly identified the error in each of the test code words."

  The prior arts of record (Arroyo et al. US 5,502,732) teach that for double bit error detection, the diagnostic bit controlling multiplexer is enabled and CPU writes a data pattern with two bits set. The ECC check bits will be calculated and stored correctly but the actual data values will be logical zeros inserted by multiplexer. When the address is read back, the ECC check bits will not

match because ECC generator placed check bits corresponding to the actual data generated by the CPU into memory and ECC generator will generate check bits based on logical zeros read back from memory along bus. Thus, the syndrome will be nonzero and indicate that a double bit error has occurred (col. 5, lines 55-66, Arroyo et al.).

The prior arts, however, do not teach introducing an error into each of the test code words in the set by substituting check bits corresponding to an unused syndrome for a correct set of check bits within each test code word, wherein each test word comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the set of test code words. Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 30 is allowable over the prior arts of record.

- Claims 31-33 are allowed because of the combination of additional limitations and the limitations listed above.
- The claim 34 recites features such as: "...providing each of a set of n data bit combinations to the error detection/correction logic, wherein each data bit combination has n bits, wherein each possible value of each data bit is present in at least one of n data bit combinations, wherein the set of n data bit combinations provided to the error detection/correction logic is a subset of a set of all data bit combinations that is possible to create using n bits; wherein in response to being provided with the set of n data bit combinations, the error detection/correction logic is configured to generate a set of check bits for each of the n data bit combinations; and wherein the host computer system is configured to compare the set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations."

  The prior arts of record (Kurihara US 4,107,649) teach an error detection circuit which comprises a shift register having a plurality of storing stages which sequentially shifts input data and feeds back output data from an output stage to desired ones of the stages, and a parity generator in which a parity signal is generated from the parity generator in accordance with the data storing state of the shift register, the parity signal is predicted from an initial value determined by the data

storing state of the shift register in its initial state, the number of input data of logic "1" provided as an input to the shift register and/or the number of output data of logic "1" provided as an output from the shift register, and wherein the parity signal derived from the parity generator is compared with the predicted parity signal in order to detect malfunction of the error detection circuit based on the result of the comparison (col. 1, lines 44-60, Kurihara). Vishlitzky et al. teach that a mass storage system features a mass storage array having a plurality of mass storage devices, such as disk drives; a storage controller for receiving and sending data from and to the storage devices; a host computer connected to a standard based communication bus for communicating data and commands with the storage controller (col. 1, lines 51-56, Vishlitzky et al.).

The prior arts, however, do not teach providing each of a set of n data bit combinations to the error detection/correction logic. The prior arts also do not teach generating a set of check bits for each of the n data bit combinations; and wherein the host computer system is configured to compare the set of check bits generated by the error correction/detection logic with a known correct set of check bits for each of the n data bit combinations. Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 34 is allowable over the prior arts of record.

- The claim 35 recites features such as: "...a method of testing error detection/correction logic, the method comprising: providing a subset of possible data bit combinations of n data bits to the error detection/correction logic, verifying the error detection/correction logic by comparing a set of check bits generated by the error detection/correction logic for each of the n data bit combinations in the subset with a set of known correct check bits; providing a first set of m+1 test code words to the error detection/correction logic, wherein a first test code word is a correct test code word and where each other test code word in the set of m+1 test code words comprises a single-bit error, wherein each test code word having a single-bit error has the single-bit error at a different bit position than each other test code word that has a single-bit error; providing a second set of test code words to the error detection/correction logic, wherein each test code word in the second set comprises an error introduced by substituting check bits corresponding to an unused

syndrome for a correct set of check bits within a correct code word, wherein each test code word in the second set comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the second set of code words."

The prior arts of record (Kurihara US 4,107,649) teach an error detection circuit which comprises a shift register having a plurality of storing stages which sequentially shifts input data and feeds back output data from an output stage to desired ones of the stages, and a parity generator in which a parity signal is generated from the parity generator in accordance with the data storing state of the shift register, the parity signal is predicted from an initial value determined by the data storing state of the shift register in its initial state, the number of input data of logic "1" provided as an input to the shift register and/or the number of output data of logic "1" provided as an output from the shift register, and wherein the parity signal derived from the parity generator is compared with the predicted parity signal in order to detect malfunction of the error detection circuit based on the result of the comparison (col. 1, lines 44-60, Kurihara).

The prior arts of record (Arroyo et al. US 5,502,732) teach that for double bit error detection, the diagnostic bit controlling multiplexer is enabled and CPU writes a data pattern with two bits set. The ECC check bits will be calculated and stored correctly but the actual data values will be logical zeros inserted by multiplexer. When the address is read back, the ECC check bits will not match because ECC generator placed check bits corresponding to the actual data generated by the CPU into memory and ECC generator will generate check bits based on logical zeros read back from memory along bus. Thus, the syndrome will be nonzero and indicate that a double bit error has occurred (col. 5, lines 55-66, Arroyo et al.).

The prior arts, however, do not teach providing a subset of possible data bit combinations of n data bits to the error detection/correction logic, verifying the error detection/correction logic by comparing a set of check bits generated by the error detection/correction logic for each of the n data bit combinations in the subset with a set of known correct check bits; providing a first set of m+1 test code words to the error detection/correction logic, wherein a first test code word is a correct test code word and where each other test code word in the set of m+1 test code words

comprises a single-bit error, wherein each test code word having a single-bit error has the single-bit error at a different bit position than each other test code word that has a single-bit error; providing a second set of test code words to the error detection/correction logic, wherein each test code word in the second set comprises an error introduced by substituting check bits corresponding to an unused syndrome for a correct set of check bits within a correct code word, wherein each test code word in the second set comprises substituted check bits corresponding to a different unused syndrome than each other test code word in the second set of code words. Hence, the prior arts of record do not anticipate nor render obvious the claimed inventions. Thus, claim 35 is allowable over the prior arts of record.

- Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Dipakkumar Gandhi
Patent Examiner